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A ZFx86–Based System Schematic Checklist

We developed this schematic checklist to assist FAEs and OEMs that design and debug products using the ZFx86 System-on-a-Chip.

Recommendations

When designing a new project using the ZFx86, we recommend that you have COM1 functional (using an RS232 driver). Doing so allows the use of the BUR console for debug purposes. With a standard COM1 port implementation, use a *Null Modem* cable to connect to a PC running a terminal emulation program such as HyperTerminal.

Set the BUR console terminal settings as follows:

- Speed 9600 baud
- 8 bit, no parity
- Handshake set to none

If you meet minimum requirements (for example, correct bootstraps, clocks connected and power applied) and bootstrap 23 (SA23 BGA R03) is pulled up, then the BUR prompt displays on the terminal screen. No other interface chips are required. Use the Z-tag interface for on board FLASH and EEPROM device upgrades, or manufacturing test purposes.

Bootstraps

Use the x86 ISA address pins as bootstraps (Switches S2 and S3 on the IDS board). Although these bootstraps have reasonable default values, most likely some changes must be made. Table 1 lists the bootstraps together with short recommendations:

Table 1. Bootstrap Settings

SA Bit	Pin #	Name	Default	Description	Recommendation
23	R03	BUR enable	0	BUR Disabled	Pull-up to start from BUR
22	T02	ZFL enable	1	ZF Logic Enabled	Use default
21	T03	USB test mode enable	0	No USB Test	Use default
20	T04	Back PCI clock source	1	Use internal source	When using an external PCI clock source be sure to connect the 33MHz clock to the PCI CLK line (U25)
19	U01	Back PCI clk div	0	Divide SYSCLK_C by one	Pull-up (divide by two) if using higher than 33 MHz SYSCLK together with internal clock source (20)

Table 1. Bootstrap Settings(Continued)

SA Bit	Pin #	Name	Default	Description	Recommendation
18	U03	Front PCI CLK DIV	0	Divide SYSCLK_C by one	Pull-up (divide by two) if you use higher than 33 MHz SYSCLK. Several reasons require this. One of which is that using this clock with higher than 33MHz clock data, corruption might occur.
17:16	16=V01 17=U02	I486 CLK MODE	11	3x SYSCLK_C	00 – 1x 01 – 2x 11 – 3x 10 – 4x
15:13	13=V03 14=V04 15=V02	I486 CLK DELAY	010	Factory default	Use default
12	W01	Boot ROM width 8/16	1	Using an 8 bit external ISA ROM	Pull-down if using 16 bit boot memory device.
11	W02	Int/ext BUR	1	Use internal BUR when Z-tag enabled	Use default
10	W03	SIO test mode	0	Test mode disabled	Use default
09	Y01	Third PCI request/ grant enable	0	Third PCI request/ grant disabled	Pull-up if you plan to use three PCI devices.
08	Y03	486 raw clock disabled	1	486 raw clock disabled	Use default
07	Y02	486 DLL enabled	1	486 DLL clock enabled	Use default
06	AA01	Derive 32KHz from 48MHz	0	Using external 32KHz crystal	Pull-up if using internal source for 32KHz signal KHZ32C_C (AF01). Derived from division of the 48MHz clock (USB_48MHZ_C [AE15]). The Real Time Clock resets its value when power off occurs
05	Y04	Derive 14MHz from 48MHz	0	Using external 14MHz crystal	Pull-up if using internal source for 14.318MHz (AF16). Derived from division of the 48MHz clock (USB_48MHZ_C [AE15]).

Note: For normal conditions you only need pull-up/down resistors to override default bootstrap setting. The recommended pull-up is a 4.7KΩ resistor and pull-down is a 2KΩ resistor. When you expect an extensive or unknown load on the ISA address lines, then use a buffered bootstrap scheme. For example, 74LCX541 buffer enabled with PRST_N signal.

Clocks

- The ZFx86 needs both SYSCLK_C (pin A20) and USB_48MHZ_C (pin AE15) to operate. In minimum configurations, you may connect the 48MHz clock to both of these pins.

- Check that SYSCLK_C and CLK MODE bootstraps [16:17] are correct. SYSCLK_C multiplied by CLK MODE should not exceed maximum allowed (64 MHz when multiplier is 1 and 128MHz in other cases).
- The IGS clock chips are highly sensitive to power supply line noise. You must use capacitors very close to the power pins to filter the power supply.
- Use the external clock for PCI's (including ZFx86), when clock lines length generates more than 2ns skew from the ZFx86 to any other PCI device.
- PCI clock should not exceed SYSCLK or SYSCLK/2 when using a SYSCLK higher than 33MHz.

SDRAM Interface

- The MA bus, MD bus, and Memory Control lines require 10Ω series termination resistors. Place the resistors close to the ZFx86 chip.

PCI Interface

- When using PCI devices, verify that all the ZFx86 processor's REQ# and GNT# lines use 10KΩ pull-up resistors, and all PCI bus control signals use 2.7KΩ pull-up resistors.
- When using pull-up on Bootstrap 9 (third PCI Request/Grant), you must use a 10KΩ pull-up resistor on REQ2_N/GNT2_N (A14). If Bootstrap 9 is not used (default), use a 10KΩ pull-down resistor on ISA input signal DRQ1 (B14). The ZFx86 contains weak internal pull-up resistors on all PCI control signals.
- When connecting PCI chips to the PCI bus, use the following address lines as ID-SEL signals paired with their appropriate interrupt:
  - PAD20 – PCI_INTA_N (INTAX)
  - PAD21 – PCI_INTB_N (INTBX)
  - PAD22 – PCI_INTC_ N (INTCX)

  Note: Be certain to use the above signal/interrupts paired only as listed.
- For detailed information about routing PCI interrupts using the ZFx86 BIOS, refer to the Routing ZFx86 PCI Interrupt document (P/N 9150-0015-00) on the ZF Micro Devices website: *http://www.zfmicro.com*

Floppy Disk Drive Interface

- Even if a floppy drive is not used, connect 4.7KΩ pull-up resistors to the Floppy interface input signals to prevent the following inputs from floating:
  - DSKCHG_N (J02)
  - INDEX_N (F03)
  - RDATA_N (J04)
  - TRK0_N (H03)
  - WRPRT_N (H02)

IDE Interface

- When using Ultra DMA, refer to the IDS schematic for the resistor values and the configuration required.
- Place a 10KΩ pull-down resistor on IDE_DATA7 (AE18) to prevent the system BIOS from assuming a drive is connected and busy during IDE auto-detect routines.
- Verify that you use the following resistors:
  - A 10KΩ pull-up resistor on IDE_INTR lines (IRQ14 and IRQ15)
  - A 1KΩ pull-up resistor on IDE_IORDY0_N line (AD22)
  - A 10KΩ pull-down resistor on IDE_DREQ0_N line (AE23)
  - A 470Ω pull-down resistor on IDE connector IO_CS16, pin 32 on standard IDE connector

Note: We recommend that you use all these pull-up/down resistor whether the IDE interface is used or not, with the exception the 470Ω resistor on the IDE connector IO_CS16.

Mouse/Keyboard Interface

- Use a ferrite (with a recommended value of 90μH, capable of carrying 1.5 amps minimum); place one between the MSGND signal and digital ground, and the KBGND signal and digital ground.
- The PS/2 interface needs no pull-up resistors when not used, as it has internal pull-ups.

Serial Ports

- When not used, add 4.7KΩ pull-up/down resistors to the following floating Serial Port inputs:
  - CTS1X (D09) and CTS2X (A06)
  - DCD1X (A10) and DCD2X (B08)
  - DSR1X (C10) and DSR2X (C08)
  - RX1 (B10) and RX2 (A07)
  - RI1X (A08) and RI2X B06)

Parallel Port

- When not used, all Parallel Port signals may be left open. When used, refer to the IDS schematic for required resistor values and configuration.

Infrared Interface

- When not used, add a 4.7KΩ pull-up resistor to IRRX (C06) signal.

Control

- Connect Power On Reset Disable, POR_DIS (B19), to GND.

USB Interface

- At the USB connector, use ferrite beads with a recommended value of 120μH on the following pins:
  - PORT1_P (AE13) and PORT1_M (AF13)
  - PORT2_P (AF14) and PORT2_M (AE14)
- Use a ferrite (with a recommended value of 90μH capable of carrying 1.5 amps minimum) placed between the USB port GND-1 and digital ground, and GND-2 signals and digital ground.
- Connect USB port pins 9, 10, 11, and 12 to chassis ground, *not* digital ground. Connect chassis ground to digital ground through a ferrite (with a recommended value of 600μH) and a 220pF capacitor in parallel.
- For ESD protection and EMI filtering, we recommend you use special filters, for example, Semtech STF201.
- When not using the USB interface, add 4.7KΩ pull-ups on the following USB Interface floating signals:
  - PORT1_P (AE13), and PORT1_M (AF13)
  - PORT2_P (AF14), and PORT2_M (AE14)
  - OVER_CUR1# (AD12), and OVER_CUR2# (AF12)

ISA Interface

- Even if you do not fully use the ISA bus interface, place 4.7KΩ pull-up resistors on all ISA Data lines (SD0...15) together with ISA_ERROR_N (AB3).
- Place 10KΩ pull-down resistors on DRQ5 (B13), and DRQ1 (B14). (However, if B14 is used as a third PCI request, then REQ2_N needs a 10KΩ pull-up resistor. Refer to bootstrap 9 information in Table 1.)
- When using the full ISA interface (that is, an ISA connector on board) ensure that you add all pull-up resistors (refer to the IDS reference design for more information).

Boot ROM/FLASH Device

- Boot device must be connected to mem_cs0 (B4).
- With 16 bit boot device, SA12 must be pulled down and care must be taken with the address bus connection to the memory device, since memory device numbering differs depending on whether byte or word are used as a base.
- You may use Xilinx XC17 series serial configuration PROM's or Atmel AT17 series serial configuration FLASH devices for power-up and failsafe routine generation. To do so, SA23 must be pulled up (boot up from BUR enabled) and code fetching starts from serial memory device connected to the Z-tag interface. Check the reference design for correct implementation.

ZFx86 Pins Voltage Tolerants

ZFx86 is 5V tolerant part except following pins:

- All Power Supply pins including V_{BAT} and the USB power supplies.
  - V_{DD_IO} and V_{DD_USB} must be 3.3V
  - V_{DD_CORE} 2.5V and V_{BAT} to 3.0V or leave open if not used
- Clock inputs:
  - 32KHZ_C (AE01)
  - 32KHZC_C (AF01)
  - USB_48MHZ_C (AE15)
  - SYSCLK_C (A20)
- USB signals:
  - PWR_EN (AE12)
  - PORT1_P (AE13) and PORT1_M (AF13)
  - PORT2_P (AF14) and PORT2_M (AE14)
  - OVER_CUR1# (AD12) and OVER_CUR2# (AF12).
- Power On Reset Disable, POR_DIS (B19)
- SDRAM interface:
  - D[0..31] (0=C24, 1=A26, 2=B26, 3=C25, 4=D24, 5=C26, 6=E23, 7=D25, 8=E24, 9=D26, 10=E25, 11=E26, 12=F24, 13=F25, 14=G23, 15=F26, 16=G25, 17=G24, 18=G26, 19=H24, 20=H25, 21=H26, 22=J24, 23=J23, 24=J25, 25=J26, 26=K25, 27=K24, 28=K26, 29=L23, 30=L24, 31 = L25)
  - SDRAM_CS0_N through SDRAM_CS3_N (0=B25,1=A25, 2=A24, and 3=B24)
  - SDRAM_DQM0_N through SDRAM_DQM3_N (0=C23,1=B23, 2=D22, and 3=A23)
  - SDRAM_WE_N (C22)
  - SDRAMCLK[0...3] (0=B22,1=A22, 2=B21, and 3=A21)
  - SDRAM_CLKE (C21)
  - SDRAM_RAS_N (C20)
  - SDRAM_CAS_N (D20)
  - MA[0..13] (0=A15, 1=C14, 2=B15, 3=C15, 4=B16, 5=A16, 6=C16, 7=B17, 8=C17, 9=A18, 10=C18, 11=B18, 12=A19, 13=D18)

Power

- Do not run switching regulators in series to produce any on-board voltages. This causes compound noise effects that can lead to system failures.